REMARKS

Claims 1-24 are pending. Only claims 3 and 18 stand rejected.

I. REJECTION OF CLAIM 18

Claim 18 recites, in part, "an error correction circuit for carrying out an error correction operation on said codeword using error correction information provided by said plurality of phase synchronizers".

The Office Action Made Final states that "incorporating an error correction in Hsieh for carrying out error correction operation on said codeword using error correction information from said plurality of comparators (phase synchronizers would have been obvious to one skill in the art in order to ensure that the received codeword is as closed as possible to the transmitted codeword".

On the other hand, Hsieh specifically and directly refutes the Examiner's allegation. Hsieh teaches a line-based compression rule so that "if a code is corrupted, it will be contained in the line containing the same. The entire line will be ***ignored***, but the rest of the image data is designed to remain unaffected." Hsieh at col. 1, lines 46-53 (emphasis added).

The motivation for a Hsieh's ***line-based*** compression rule is so that corrupted codes can be contained in a single line and then ***ignored***. The Examiner is strenuously urged to re-read the entire paragraph starting at Hsieh at col. 1, line 40. Note also that the following paragraph states that the run-length compression method (described throughout Hsieh) is a popular line-based compression method.

Also note the entire paragraph starting at Hsieh at col. 1, line 23. Note the emphasis on achieving "real-time or near-real-time decoding". "In order to achieve real-time or near-real-time decoding, the decoding algorithm must be relatively simple, and must be done on a sequential basis." Hsieh at col. 1, lines 34-36. This is the Hsieh's motivation for ***ignoring*** (as opposed to ***error correcting***) a line with corrupted codes.

Ignoring corrupted codes and displaying only the uncorrupted lines clearly teaches away from ***an error correction operation*** as set forth in claim 18

The teachings of Hsieh cannot be ***ignored***. The teachings of Hsieh cannot be ***corrected*** by citing a patent document that allegedly makes up for the teaching deficiencies of Hsieh since Hsieh teaches away from the alleged teachings of the patent document.

In fact, not only does Hsieh teach away from the alleged teachings of the other patent document, Hsieh teaches away from the claimed invention as set forth in claim 18.

It is respectfully requested that the rejection be withdrawn with respect to claim 18.

II. REJECTION OF CLAIM 3

Claim 3 recites, in part, "an input shift register for receiving a sequence of bits comprising a codeword; a plurality of phase synchronizers associated with a corresponding plurality of potential phases of said codeword, each of said phase synchronizers producing a codeword valid signal upon determining that said input shift register includes a set of said bits corresponding to said codeword".

Applicant argued that the Code Comparators of Hsieh do not correspond with a plurality of potential phases of a codeword. Each Code Comparator of Hsieh receives a different codeword and not potential phases of a particular codeword. The codewords received by each Code Comparator of Hsieh are different because the shifter has reset a first portion of bits to zero, if application, for respective Code Word Comparators. See, e.g., col. 8, lines 48-54 of Hsieh. These are not different phases of the same codeword, but actually different codewords of possibly variable length due to the forced reset of the first portions.

In response, the Examiner points to the specification at paragraph 0022 at lines 7 and 8. "Specifically, each phase synchronizer 70 examines a different 64-bit sequence of the serially received data (i.e., a different potential codeword phase) in an effort to determine whether such sequence corresponds to a valid codeword in the manner described hereafter". Specification at paragraph 0022 at lines 7-10 (describing part of one embodiment according to one or more aspects of the present invention).

From this singular quote, the Examiner logically and presumably makes a few extrapolations:

(1) first, the Examiner may be concluding that "a different 64-bit sequence of the serially received data" is defined as "a different potential codeword phase";

(2) second, the Examiner may be extrapolating that "a different 64-bit sequence of the serially received data" and "a different potential codeword phase" are the same as a the Examiner's phrase "different code word sequence";

(3) third, the Examiner may be further extrapolating that the Examiner's phrase a "***different code word sequence***" is the same as Applicant's argued phrase "***different codeword***"; and

(4) fourth, the Examiner may be yet further extrapolating that a "different codeword" of Hsieh means the same as a "plurality of potential phases of said codeword" as set forth in claim 3.

It is believed that the full extrapolation of logic is relatively tenuous and cannot be supported by the specification at cited paragraph 0022. One of the problems in the logical extrapolations of the Examiner appears to be the equating of a "different code word sequence" with a "different codeword". "Different code word sequence" does not necessarily mean "different codeword". Applicant respectfully requests that the Examiner re-read the entire paragraph 0022. According to part of one embodiment according to one or more aspects of the present invention, each phase synchronizer 70 examining a different 64-bit sequence of serially received data can be explained as follows: phase "0" synchronizer 70 examines received bits K through K+63, then phase "1" synchronizer 70 would examine received bits K+1 through K+64, the phase "2" synchronizer 70 would evaluate received bits K+2 through K+65, and so on. See specification at paragraph 0022 at lines 10-13. Thus, the specification at paragraph 0022 describes that each synchronizer examines a different 64-bit sequence of serially received data without there necessarily being any support provided that each synchronizer corresponds to a different code word.

For at least the above reasons, the evidence cited by the Examiner does not support the proposed definitions and extrapolations by the Examiner.

It must be noted that Applicant is not attempting to import any limitations from the specification to the elements as set forth in claim 3. Applicant neither agrees nor disagrees with the Examiner's characterization of the alleged prior art or the elements as set forth in claim 3. Instead, Applicant has merely pointed out that the specific evidence that the Examiner alleges in a specifically cited section of the specification does not appear to support the Examiner's

conclusion which is the basis for the rejection of claim 3. Applicant is in no way limiting the scope or characterization of the elements as set forth in claim 3 in view of, for example, cited paragraph 0022 of the specification.

It is respectfully requested that the rejection be withdrawn with respect to claim 3.

III. CONCLUSION

In view of at least the foregoing, it is respectfully submitted that claims 1-24 are in condition for allowance. Should anything remain in order to place the present application in condition for allowance, the Examiner is kindly invited to contact the undersigned at the below-listed telephone number.

Please charge any required fees not paid herewith or credit any overpayment to the Deposit Account of McAndrews, Held & Malloy, Ltd., Account No. 13-0017.

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Respectfully submitted,

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